REMARKS

Claims 1-34 are currently pending in the subject application and are presently under consideration. Claims 1, 23, 33, and 34 have been amended to more clearly recite aspects of the invention. Claims 2 and 28 have been canceled herein without prejudice or disclaimer. Claims 3-10, 26, and 29-32 have been amended to correct dependencies. Accordingly, no new matter has been introduced, no new search is required, and it is respectfully submitted that the amendments should be entered. Favorable reconsideration of the subject patent application is respectfully requested in view of the amendments and comments herein.

I. Rejection of Claims 1-11, 14, 19-34 Under 35 U.S.C. §102(e)

Claims 1-11, 14, 19-34 stand rejected under 35 U.S.C. 102(e) as being anticipated by Auschnitt *et al.* (U.S. App. 2005/0105092). Withdrawal of this rejection is requested for at least the following reasons. Auschnitt *et al.* does not disclose all limitations of the subject claims.

> A single prior art reference anticipates a patent claim only if it expressly or inherently describes each and every limitation set forth in the patent claim. *Trintec Industries, Inc. v. Top-U.S.A. Corp.*, 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the ... claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant's invention generally relates to a multi-layer overlay measurement and correction technique for integrated circuit manufacturing. Independent claims 1, 23, 33, and 34 recite similar limitations, namely, a measurement component that generates images/signatures of an overlay target, a comparison component that compares the images/signatures of the overlay target with one or more stored images/signatures, and ***a control component or correction of overlay error step*** that utilizes the overlay error determined by the measurement component to correct overlay error between the three or more layers of the wafer.

Auschnitt *et al.* generally relates to an overlay target and ***measurement method*** using reference and sub-grids. Independent claims 23, 37, 38, 39, and 40 recite similar limitations, namely, ***methods for determining alignment error*** in electronic substrates that comprise providing a first grid pattern on a layer of a substrate, providing nested within the first grid

pattern a second contrasting set of elements, measuring location of the first set of elements in the first grid pattern, determining the center of the first set of elements in the first grid pattern, measuring location of the second set of elements in the second grid pattern, determining the center of the second set of elements in the second grid pattern, and comparing the center of the first set of elements and the center of the second set of elements and determining alignment error.

The Examiner contends that Auschnitt *et al.* discloses an overlay target that represents overlay between three or more layers of a wafer (Fig. 4), and a measurement component (Fig. 2-14) that determines overlay error existent in the overlay target, and thereby determines overlay error between the three or more layers of the wafer, where the measurement component comprises a comparison component that compares a captured signature with one or more stored signatures to determine overlay error existent in the overlay target (para. [0003], [0008]-[0009], [0020], [0045]-[0046], and Fig. 4-14). The Examiner further contends that Auschnitt *et al.* discloses ***a control component*** that utilizes the overlay error determined by the measurement component to correct overlay error between the three or more layers of the wafer (Fig. 4), wherein the control component provides more correction in a first dimension and less correction in a second dimension in an instance in which design rule requirements tolerate less overlay error in the first dimension when compared to the second dimension (para. [0003], [0006], [0008], Fig. 9-14).

Auschnitt *et al.* does not disclose ***a control component or correction of overlay error step*** that utilizes the overlay error determined by the measurement component to correct overlay error between the three or more layers of the wafer, as recited in independent claims 1, 23, 33, and 34. The cited paragraphs and figures only disclose ***a method for measuring overlay error*** in the fabrication of integrated circuits. The cited paragraphs and figures are addressed in turn.

Paragraph [0003] describes general background associated with overlay error measurement. Specifically, paragraph [0003] describes a method for measuring overlay error well known to those in the art; namely, using overlay targets of nested sub-patterns printed together with the functional circuit elements at each successive lithographic step, generating images of the overlay targets that are captured by an imaging system, and using an algorithm to extract the relative displacement of the nested sub-patterns. There is no disclosure of ***a control***

component or correction of overlay error step that utilizes the overlay error determined by the measurement component to correct overlay error between the three or more layers of the wafer.

Paragraph [0006], also located in the description of the general background of the invention of Auschnitt *et al.*, generally describes problems to be addressed by the invention of Auschnitt *et al.*. Paragraph [0006] describes the constraints associated with the ideal overlay target. Without going into exhaustive detail, paragraph [0006] discloses features related to an overlay target, not a ***control component or correction of overlay error step*** in accordance with the subject invention.

Paragraph [0008] summarizes an overlay target that is an object of the invention of Auschnitt *et al.* Briefly, paragraph [0006] discloses an overlay target with various features, and none of the disclosed features relate to a control component or correction of overlay error step as disclosed in the subject invention. The most relevant feature of the disclosure with respect to the subject invention relates to enabling *in situ* compensation for imaging system distortion. This disclosure relates to imaging system correction measures, not ***a control component or correction of overlay error step***.

Furthermore, none of Figs. 9-14 disclose ***a control component or correction of overlay error step*** in accordance with the subject invention.

In sum, Auschnitt *et al.* cannot disclose ***a control component or correction of overlay error step*** because Auschnitt *et al.* solely relates to an overlay target and ***a method for determining overlay error*** in the fabrication of an integrated circuit. As such, the overlay target and method disclosed by Auschnitt *et al.* are silent with respect to the ***control component or correction of overlay error step*** recited in independent claims 1, 23, 33, and 34 of the subject invention. Accordingly, the applicants' representative respectfully requests this rejection be withdrawn.

II. Rejection of Claims 1-7, 9-11, 13-20, 22-34 Under 35 U.S.C. §102(b)

Claims 1-7, 9-11, 13-20, 22-34 stand rejected under 35 U.S.C. §102(b) as being anticipated by Tsuchiya *et al.* (U.S. 6204912). Withdrawal of this rejection is requested for at least the following reasons. Tsuchiya *et al.* does not disclose all limitations of the subject claims.

Tsuchiya *et al.* generally relates to an exposure method, an exposure apparatus, and a mask that are suitable for manufacturing an active matrix liquid crystal display having a

switching device. Specifically, a ***stitching portion*** between unit patterns in a second layer is offset from the ***stitching portion*** in a first layer by a predetermined distance. Accordingly, Tsuchiya *et al.* applies to ***stitching portions***, not ***overlay targets***. Tsuchiya *et al.* is silent with respect to an ***overlay target***.

A ***stitching portion*** is not an ***overlay target***. Tsuchiya *et al.* describes ***stitching portions*** as boundaries between successively exposed unit patterns. *See* col. 2, ll. 8-17. Alternatively, Tsuchiya *et al.* describes ***stitching portions*** as "the area in which two projection areas are overlapped during exposure[.]" *See* col. 3, ll. 6-43. Consequently, a ***stitching portion*** is a boundary between successively exposed unit patterns; a ***stitching portion*** is not an element of defined shape or series of shapes deposited in successive layers in order to track overlay error during integrated circuit fabrication.

An ***overlay target*** is an element deposited with the integrated circuit components, with a defined shape or a defined series of shapes. As subsequent layers are deposited, rotation and/or translation (*i.e.*, overlay error) of the ***overlay target*** can be tracked in order to determine overlay error. An ***overlay target*** is not the boundary between successively exposed unit patterns within a single layer.

Independent claims 1, 23, 33, and 34 contain the limitation of an ***overlay target***, and because Tsuchiya *et al.* refers only to ***stitching portions***, Tsuchiya *et al.* is silent with respect to ***overlay targets***. Consequently, Tsuchiya does not teach or suggest each and every feature of the subject claims. Applicants' representative respectfully requests withdrawal of this rejection.

III. Rejection of Claims 1-34 Under 35 U.S.C. §102(e)

Claims 1-34 stand rejected under 35 U.S.C. §102(e) as being anticipated by Mieher *et al.* (U.S. App. 2004/0257571). Withdrawal of this rejection is requested for at least the following reasons. Mieher *et al.* does not disclose all limitations of the subject claims.

Mieher *et al.* generally relates to apparatus and methods for detecting overlay errors using scatterometry. Independent claim 1 recites a method of determining an overlay error between two layers of a multiple layer sample, the method generally comprising measuring a first optical signal from a plurality of first periodic targets and a second optical signal from a second structure, and determining an overlay error between the first and second structures by analyzing the periodic targets using a scatterometry overlay technique based on predefined offsets.

The Examiner contends that Mieher *et al.* anticipates claims 1-34. Specifically, the Examiner contends that Mieher *et al.* discloses a control component (or corrective step) that utilizes an overlay error determined by a measurement component to correct overlay error. The applicants' representative respectfully disagrees for at least the following reasons. Mieher *et al.* discloses apparatus and methods for detecting overlay errors using scatterometry, but Mieher *et al.* is silent with respect to ***a control component or correction of overlay error step***, a limitation included in independent claims 1, 23, 33, and 34 of the subject invention.

Like Auschnitt *et al.*, Mieher *et al.* limits itself to ***apparatus and methods for detecting overlay errors*** using scatterometry. For example, Fig. 3(a) is described as "a flow diagram illustrating a procedure . . . for determining overlay in accordance with one embodiment of the present invention." *See* para. [0077]. The flow diagram depicted in Fig. 3(a) comprises: 1) two pairs of measurements (*e.g.*, "Measure target A," "Measure target B," *etc.*) which are followed by 2) two spectra substractions (*e.g.*, "(S_A-S_B)" and "(S_C-S_D)") which is followed by 3) obtaining properties of the difference spectra ultimately leading to 4) calculating overlay based on function. *See* Fig. 3(a). The flow diagram stops with calculating overlay error. No ***control component or correction of overlay error step*** is disclosed.

For the reasons similarly concerning the subject invention's limitation of ***a control component or a correction of overlay error step*** laid forth in Section I of this Reply, the applicants' representative respectfully requests this rejection be withdrawn.

CONCLUSION

The present application is believed to be in condition for allowance in view of the above comments and amendments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [AMDP986US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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